PRODUCING PLANARIZED UNIFORM LAYER IN ADVANCED PHOTOSENSITIVE POLYIMIDE OVER COMPLEX GEOMETRY FOR FAN OUT PLP APPLIED WITH A NOVEL NOZZLE-LESS SPRAY COATING TECHNOLOGY

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ABSTRACT
With growing demand for advanced computing systems and as personal handheld devices become more powerful, front-end manufacturers are required to reduce the physical footprint of and at the same time integrate more functionality into their chips. More I/O channels are packed into smaller areas than ever before in modern packages. The competing demands of increasing throughput and reducing costs makes the interconnection of these packages increasingly challenging. New methods to produce these high-density interconnections are required to meet these challenges.

Chips are placed and connected both horizontally and vertically in 2.5D and 3D packaging. This created inherent topographical challenges for producing the interconnections. The industry's drive for cost reduction is building momentum toward more efficient and cost effective methods for creating the multi-layer high density interconnects. There are inherent topographical challenges associated with the growth of 2.5D and 3D packaging where chips are placed and interconnected horizontally and vertically. One critical area of interest is the formation of the passivation layer that enables connections between layers. Polyimides must be applied in a uniform layer to ensure that the inter-layer connections can properly be formed. Effectiveness of different film deposition methods is measured in terms of formation of uniform and void-free films to ensure intended mechanical and electrical integrity of the material is not compromised. Film deposition method can potentially influence not only film density but also polymer chain configuration that control key properties directly linked to the reliability of the material. While polarity of functional groups dictates moisture uptake, polymer chain configuration can control moisture permeability through the deposited film and its ability to act as corrosion barrier.

We have previously reported creation of high-density vias printed in a dielectric film deposited by a revolutionary technique in the form of a novel nozzle-less ultrasonic spray technology. [1] This paper presents impact of such unique deposition method on key film properties like density and moisture permeability along with supporting reliability data under high temperature storage (HTS) and unbiased-HAST conditions. Other key performance parameters like filling and planarization over complex topography of an advanced dielectric material will be compared and analyzed for this approach against other liquid film deposition techniques.

Keywords:-nozzle-less spray; Passivation Laver; PLP; WLP; panel; wafer; advanced packaging; stepper; polyimide

INTRODUCTION
Demand for more functionality and power in electronic devices continues unabated and will certainly continue into the future. Handheld personal devices, wearables, IoT devices, and even automotive components are all contributing to this momentum. This increased performance demand is accompanied by a seemingly conflicting goal of also reducing the form factor of these modern devices. With front-end-of-line (FEOL) approaching the absolute limits of what can be packed into a chip, it has fallen to the back-end-of-line (BEOL) to shoulder this burden.

Advanced packaging is one of the main BEOL suites of technologies where significant gains are still being made. Through the interfacing of chips coming from the FEOL, dedicated packages can be manufactured to meet the performance and dimensional requirements of today's electronics.

Traditionally, advanced packaging has been a predominantly wafer-centric affair, in fan-out wafer level packaging (FOWLP), silicon wafers are diced and reassembled on reconstituted wafers to allow for the redistribution of their I/O channels to other locations and/or chips. In recent years, though, driven in part by the constant need to increase yields and lower cost, panel-level