PRODUCING VIAS IN PHOTOSENSITIVE POLYIMIDE PASSIVATION LAYERS FOR FAN OUT PLP THROUGH THE INTEGRATION OF AN ADVANCED LITHOGRAPHY SYSTEM WITH A NOVEL NOZZLE-LESS SPRAY COATING TECHNOLOGY

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***Abstract*—As demand for ever more powerful personal handheld devices and advanced computing systems continues to grow, front-end manufacturers have pushed Moore's Law to the limit and integrated more functionality into their chips while at the same time reducing their physical footprint. Modern chips now contain more I/O channels in smaller areas than ever before. The interconnection of these devices has become more challenging along with competing demands to reduce costs and increase throughput. New methods are required to meet these challenges.**

There are inherent topographical challenges associated with the growth of 2.5D and 3D packaging where chips are placed and interconnected horizontally and vertically. The industry's drive for cost reduction is building momentum toward more efficient and cost effective methods for creating the multi-layer high density interconnects. One critical area of interest is the formation of the passivation layer that enables connections between layers. Polyimides must be applied in a uniform layer to ensure that the inter-layer connections can properly be formed.

This paper demonstrates the feasibility of a revolutionary technique in the form of nozzle-less ultrasonic spray technology in conjunction with a next generation advanced packaging lithographic system for the creation of high-density vias. Performance parameters including polyimide thickness uniformity, and CDU will be compared and analyzed for this approach against other liquid film application methods. Results from the examination of the efficacy, cost reduction potential of this novel method for high-volume manufacturing will be presented.

Keywords-*nozzle-less spray; Passivation Laver; PLP; WLP; panel; wafer; advanced packaging; stepper; polyimide*

I. INTRODUCTION

Demand for more functionality and power in electronic devices continues unabated and will certainly continue into the future. Handheld personal devices, wearables, IoT devices, and even automotive components are all contributing to this momentum. This increased performance demand is accompanied by a seemingly conflicting goal of also reducing the form factor of these modern devices. With front-end-of-line (FEOL) approaching the absolute limits of what can be packed into a chip, it has fallen to the back-end-of-line (BEOL) to shoulder this burden.

Advanced packaging is one of the main BEOL suites of technologies where significant gains are still being made. Through the interfacing of chips coming from the FEOL, dedicated packages can be manufactured to meet the performance and dimensional requirements of today's electronics.

Traditionally, advanced packaging has been a predominantly wafer-centric affair, in fan-out wafer level packaging (FOWLP), silicon wafers are diced and reassembled on reconstituted wafers to allow for the redistribution of their I/O channels to other locations and/or chips. In recent years, though, driven in part by the constant need to increase yields and lower cost, panel-level packaging has become an attractive alternative with a growing